Lab Description

In the test bench file, I just first reset the value and then test it from X=0 to pass the state from the initial to our final state and then change the input to 1 to see if the state goes back to the S0. As my expectation, the Q1 and Q0 changes from 00 to 01 and then cycled once and then increased the state one by one from 01 to 11 and cycled back to 01 which corresponds to the state machine I draw. It fully indicates that my Verilog code is correct.